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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,525	03/08/2002	Keishiro Okamoto	020214	3829

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EXAMINER	
GEBREMARIAM, SAMUEL A	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 02/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/092,525	OKAMOTO ET AL.
	Examiner	Art Unit
	Samuel A Gebremariam	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: The phrase "a capacitors" appears to be incorrect. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-4, 5, 6, 8-9, and 13-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamauchi et al. US patent No. 6,503,778.

Regarding claim 1, Yamauchi teaches (figs. 1, and 3A-27B) a semiconductor apparatus, comprising: a support substrate (11) having through holes (col. 6, lines47-67) filled with conductor in conformity with a first pitch, capacitors (20, col. 18, lines 53-61) formed on the support substrate (11), a wiring layer (27a-27c) formed on the support, leading some of the through holes filled with conductor upwards via the capacitor (20), having branches (see fig. 4a-4d), and having wires of a second pitch (29a-29c), different from the first pitch, and semiconductor element (8) disposed on the wiring layer (29a-29c), having terminals (38a, 38b) in conformity with the second pitch, and connected with the wiring layer via the terminals.

Yamauchi inherently teaches the limitation that the semiconductor element disposed on the wiring layer having terminals in conformity with the second pitch with the wiring layer via the terminals since making connection between devices requires electrical connection between terminals that conform to each other.

Regarding claim 2, Yamauchi teaches the entire claimed structure of claim 1 above including a circuit board having wiring of a first pitch and connected to lower surfaces of the through holes fills with conductor.

Yamauchi teaches (col. 3, lines 41-51) an integrated circuit or a plurality of device layers with circuit elements. Integrated circuits often involve the use of circuit boards in order to integrate different device elements. This often involves forming contacts to wires and contact holes. Therefore Yamauchi inherently teaches circuit boards having wiring layers with a pitch.

Regarding claim 3, Yamauchi teaches the entire claimed structure of claim 1 above including that the second pitch is narrower than the first pitch (refer to the middle fig. 4D, where it is shown that 27c is wider than 29c).

Regarding claims 4 and 5, Yamauchi teaches (fig. 1) the entire claimed structure of claim 1 above including the support substrate is a Si substrate (11) having through holes (col. 4, lines1-11) with an insulation film (26 and 28) formed on the side walls of the holes, and the through holes filled with conductor are metallic conductors packed in the through holes.

Regarding claim 6, Yamauchi teaches (figs. 1 and 4c, col. 6, lines 47-58) the entire claimed structure of claim 1 above including the insulation film is a silicon oxide

film and lower surfaces of the silicon substrate are also covered with an insulating material.

With regard to the limitation that the silicon oxide film is formed by thermal oxidation is not given patentable weight because, this is considered a product-by-process claim. "[E]ven though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Regarding claims 8 and 9, Yamauchi teaches (1) the entire claimed structure of claim 1 above including the through holes filled with conductor (27a-27c) include a first signal wire the wiring layer contains a second signal wire (29a-29c) for leading the first signal wire substantially vertically; and the capacitor has electrodes (inherent characteristics of a capacitor) with a vacancy (region between 29a, 29b and 29c) around a region where the second signal wire is located.

Regarding claim 13, Yamauchi teaches (figs. 4a-4d) the entire claimed structure of claim 1 above including the wiring layer contains a wiring connecting the plural semiconductor elements with each other.

Regarding claim 14, Yamauchi teaches (figs. 4a-4d) the entire claimed structure of claim 1above including another circuit part connected with the wiring layer.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi.

Regarding claim 10, Yamauchi teaches (figs. 4a-4d) the entire claimed structure of claim 1 above except explicitly stating that the insulation layer disposed on the support substrate, have a thermal expansion coefficient of 10 ppm/°C or less in the in-plane direction, and insulates the wiring layer and the capacitor.

Parameters such as coefficient of thermal expansion and heat capacity in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the thermal expansion coefficient of Yamauchi structure as claimed in order to improve the thermal property of the device.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi in view of Kabumoto et al. US patent No. 5,883,428.

Regarding claim 7, Yamauchi teaches (fig. 1) the entire claimed structure of claim 1 above except explicitly teaching that the capacitor is a decoupling capacitor connected between power wires.

Decoupling capacitors are conventional in the art and are also taught by Kabumoto (fig. 1) for reducing power-supply noise (col. 5, lines 23-48).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the decoupling capacitors taught by Kabumoto in the structure of Yamauchi in order to reduce noise between the power wires of Yamauchi's integrated device.

6. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi in view of Cuchiaro et al. US patent No. 5,888,585.

Regarding claims 11 and 12, Yamauchi teaches the entire claimed structure of claim 1 above except explicitly stating that the capacitor has a capacitor dielectric layer made of an oxide containing at least one of Ba, Sr and Ti, and a pair of capacitor electrodes sandwiching the capacitor dielectric layer and containing at least partially one of Pt, Ir, Ru, Pd or any of their oxides.

Cuchiaro teaches a charge storage device including high dielectric material comprising barium and platinum electrode in the process of making an integrated device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the capacitor structure of Yamauchi device using the materials taught by Cuchiaro in order to form a capacitor structure that is smaller in size and less leakage current.

Response to Arguments

7. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References C and D are cited as being related to semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is (571)-272-1653. The examiner can normally be reached on 8:00am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
February 9, 2004

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800